Attorney Docket No.: P-5691-US

APPLICATION FOR UNITED STATES PATENT

FOR

METHOD AND APPARATUS TO GENERATE SIGNALS USING TWO OR MORE PHASE LOCKED LOOPS

INTEL REFERENCE NO.: P16078

EPL&C REFERENCE NO: P-5691-US

Inventor: REUVEN, Yossef

Prepared by: Moshe Vegh

Intel Corporation

94 Em-Hamoshavot Way.

Ezorim Park, Building 2

Petach-Tikva 49527

Israel

Phone: (972) 3 9207513

Facsimile: (972) 3 9207509

METHOD AND APPARATUS TO GENERATE SIGNALS USING TWO OR PHASE LOCKED LOOPS

BACKGROUND OF THE INVENTION

[001] Transmitters and/or receivers of wireless communication systems such as, for example, a cellular radio communication system, wireless local area network (WLAN) and the like, may include two or more synthesizers that may be used to receive and/or transmit two or more signals, respectively. The two or more signals may have substantially the same frequency. Transmitters and/or receivers having two or more synthesizers may include a circuit to synchronize the output frequencies of the output signals provided by the two or more synthesizers. Each of the two or more synthesizer may be embedded in a single integrated circuit (IC). Thus, at least two ICs and a synchronization unit may be required in order to provide two output signals having substantially the same frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

[002] The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanied drawings in which:

[003] FIG. 1 is a schematic illustration of a wireless communication system according to an exemplary embodiment of the present invention; and

[004] FIG. 2 is a block diagram of a radio device according to some exemplary embodiments of the present invention.

[005] It will be appreciated that for simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION OF THE INVENTION

[006] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However it will be understood by those of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to obscure the present invention.

[007] Some portions of the detailed description, which follow, are presented in terms of algorithms and symbolic representations of operations on data bits or binary digital signals within a computer memory. These algorithmic descriptions and representations may be the techniques used by those skilled in the data processing arts to convey the substance of their work to others skilled in the art.

[008] Unless specifically stated otherwise, as apparent from the following discussions, it is appreciated that throughout the specification discussions utilizing terms such as "processing," "computing," "calculating," "determining," or the like, refer to the action and/or processes of a computer or computing system, or similar electronic computing device, that manipulate and/or transform data represented as physical, such as electronic, quantities within the computing system's registers and/or memories into other data similarly represented as physical quantities within the computing system's memories, registers or other such information storage, transmission or display devices. In addition, the term "plurality" may be used throughout the specification to describe two or more components, devices, elements, parameters and the like. For example, "plurality of mobile stations" describes two or more mobile stations.

[009] It should be understood that the present invention may be used in a variety of applications. Although the present invention is not limited in this respect, the circuits and techniques disclosed herein may be used in many apparatuses such as transmitters and/or receivers of a radio system. Transmitters and/or receivers intended to be included within the scope of the present invention may be included, by way of example only, within a wireless local area network (WLAN), two-way radio communication system, digital communication system, analog communication system transmitters, cellular radiotelephone communication system, and the like.

[0010]Types of cellular radiotelephone communication system intended to be within the scope of the present invention include, although are not limited to, Wideband Code Division Multiple Access (WCDMA), Global System for Mobile communication (GSM), General Packet Radio Service (GPRS), extended GPRS extended data rate for global evolution (EDGE), and the like.

[0011]Turning to FIG. 1, a wireless communication system 100 in accordance with exemplary embodiment of the invention is shown. Although the scope of the present invention is not limited in this respect, wireless communication system may include at least one base station (BS) 110 and at least one mobile station 120. In this exemplary embodiment of the invention, MS 120 may include a dual output synthesizer 130, a transceiver 140 and antennas 150 and 160.

[0012]Although the scope of the present invention is not limited in this respect, types of antennas that may be used for antenna 150 and/or antenna 160 may include an internal antenna, a dipole antenna, an omni-directional antenna, a monopole antenna, an end fed antenna, a circularly polarized antenna, a micro-strip antenna, a diversity antenna and the like.

[0013]Although the scope of the present invention is not limited in this respect, in some embodiments of the invention, dual output synthesizer 130 may include a fractional N synthesizer and a constant division synthesizer. In such embodiments, for example, the fractional N synthesizer may provide a signal with a desired frequency to a first output of dual synthesizer 130. In addition, the fractional N synthesizer may provide at least a portion of the signal to the constant division synthesizer, if desired. The constant division synthesizer may use this signal to provide a second signal to the second output of dual synthesizer 130.

[0014]Although the scope of the present invention is not limited to this embodiment, dual synthesizer 130 may provide at least two signals to transceiver 140. For example, transceiver 140 may include at least one GSM receiver and transmitter and synthesizer 140 may provide signals that may be used by transceiver 140 to transmit and receive signals through antennas 150 and 160, if desired. It should be understood by persons skilled in the art that transceiver 140 may include any suitable type of cellular transceiver or WLAN transceiver or two-way radio transceiver or digital radio transceiver and the like.

[0015]Turning to FIG. 2, a schematic block diagram of a radio device 200 according to an exemplary embodiment of the invention is shown. Although the scope of the present invention is not limited in this respect, radio device 200 may include a dual output synthesizer 300 and a transceiver 250 to transmit and/or receive signals from antennas 260 and 270. Transceiver 250 may include mixers 220 and 230 and low noise amplifiers (LNA) 240 and 245. In some exemplary embodiments of the present invention, radio device 200 may include a fractional N synthesizer 310 and an integer division synthesizer 350, as described below, both of which synthesizers may be included in dual output synthesizer 300, if desired.

[0016] Although the scope of the present invention is not limited in this respect, dual output synthesizer 300 may include an oscillator 305, for example, a crystal oscillator, or any other suitable type of oscillators. Oscillator 305 may be used to provide a fundamental frequency to fractional N synthesizer 310. Fractional N synthesizer 310 may provide an output signal 345 with a desired frequency. Output signal 345 may be provided to integer division synthesizer 350, and the frequency of output signal 345 may be used as a fundamental frequency for integer division synthesizer 350.

[0017]In some embodiments of the invention, fractional N synthesizer 310 may include a fractional N divider 320, a phase locked loop (PLL) 330 and a voltage controlled oscillator (VCO) 340. Although the scope of the present invention is not limited in this respect, fractional N synthesizer 310 may be any fractional N synthesizer known to persons skilled in the art. For example, fractional N divider 320 may include other components (not shown) such as, for example, a serial data interface, registers, latches, a reference signal divider to divide the signal of crystal oscillator 305, an accumulator, a digital to analog converter (DAC), dual modulus pre-scalar divider and the like.

[0018] Although the scope of the present invention is not limited in this respect, fractional N synthesizer 310 may generate output signal 345 with the desired frequency. In this embodiment, fractional N divider 320 may divide a frequency provided by VCO 340 by N, wherein N may be a rational fraction of integers M and L, i.e., $N=M/L$, wherein $0<M<L$, such that $0<N<1$. PLL 330 may set the frequency of output signal 345 by controlling the voltage of VCO 340. PLL 330 may include a phase detector (not shown) to lock the phase of the desired frequency. PLL 330 may

vary the voltage of VCO 340 according to the detected phase. Accordingly, VCO 340 may provide output signal 345 at the desired frequency, which may be set by PLL 340.

[0019] Although the scope of the present invention is not limited in this respect, the frequency of output signal 355 may be derived from the frequency of output signal 345. In some embodiments of the present invention, at least a portion of output signal 345 may be provided as input to an integer divider 360 of integer synthesizer 350. In some of those embodiments, integer divider 360 may divide the frequency of output signal 345 by one, such that the frequency of output signal 355 of integer synthesizer 350 may be substantially the same as the frequency of output signal 345, which may be the desired frequency. In other embodiments of the invention, integer divider 360 may divide the frequency of output signal 345 by an integer greater than one, for example, 2, 4, 9, 15 and the like, such that the frequency of output signal 355 may be a fraction of the frequency of output signal 345.

[0020] Although the scope of the present invention is not limited in this respect, integer division synthesizer 350 may include a PLL 370 and VCO 380. PLL 370 may receive output signal 345 of VCO 340 and may control VCO 380 to provide output signal 355 substantially at the same frequency as that of output signal 345. PLL 370 may include a phase detector (not shown). Integer divider 360 may provide a desired frequency to PLL 370. The phase detector may detect and lock a phase of the desired frequency and PLL 370 may vary a voltage of VCO 380 to provide the desired frequency of output signal 355.

[0021] Although the scope of the present invention is not limited in this respect, in an exemplary embodiment of the invention output signals 345 and 355 may be provided as inputs to mixers 220 and 230 of transceiver 250, respectively. In this exemplary embodiment of the invention, signals 345 and 355 may be used to upconvert or downconvert transmitted and/or received signals from antennas 260 and 270, respectively. For example, two signals of the same frequency from different paths may be received simultaneously by antennas 260 and 270, respectively, and the signals may be downconverted to corresponding baseband signals by mixers 220 and 230.

[0022] Although the scope of the present invention is not limited in this respect, antenna 260 may receive a signal, which may be amplified by LNA 240 and input to a mixer 220. Mixer 220 may mix output signal 345 to provide downconverted signal 225, if desired. Antenna 270 may receive a signal, which may be amplified by LNA 245 and input to a mixer 230. Mixer 230 may mix output signal 355 to provide downconverted signal 235, if desired. It should be understood by persons skilled in the art that signals 225 and 235 may be downconverted to the baseband frequency and/or baseband signals may be upconverted to the transmission frequency, if desired. In other embodiments of the invention, signals 225 and 235 may be further processed, e.g., to enhance performance parameters of radio device 200, if desired.

[0023] Although the scope of the present invention is not limited in this respect, in some embodiments of the invention, PLL 330 and/or VCO 340 and/or PLL 370 and/or VCO 380 may not be included in synthesizers and may be controlled by a controller or processor, if desired.

[0024] While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.